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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/826,405	04/03/2001	Rodney T. Burt	0437-A-250	2940

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EXAMINER

ABRAHAM, ESAW T

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 01/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/826,405

Applicant(s)

BURT ET AL.

Examiner

Esaw T Abraham

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-- The MAILING DATE of this communication appears on the cover sheet with the corresponding address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 April 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-35 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☒ Notice of Draftperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2. 6) ☐ Other: _____

DETAILED ACTION

1. Claims **1 to 35** are presented for examination.

Information Disclosure Statement

2. The examiner has been considered the references listed in the information disclosure statement submitted on 04/03/01.

Drawings

3. The **drawings** are objected to because of the problems addressed in the attached PTO-948. Correction is required.

Claim objections

4. Claim 1 is objected to because of the following informalities:

Please change the phrase “capable of calibrating ” to “for calibrating” (in claim 1 line 3).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim **35** is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are:

It is not clear where in the claimed language “high voltage difference amplifier circuit” of claim 35 related to claim 32. The interconnection of the claims is not understood for proper examination.

Claim Rejections - 35 USC § 103

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The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
6. Claims 1-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dudziak et al. (U.S. PN: 4,847,569) in view of Bickley et al. (U.S. PN: 6,088,581)

As per claims 1 and 29, Dudziak et al. teach or disclose a signal generator including a calibration circuit for providing periodic recalibration of the generator and a reference frequency source for producing a fixed frequency signal (see abstract). Further Dudziak et al. disclose an oscillator (VCO) for producing a variable frequency signal in accordance with a voltage input to the oscillator and an adjustable dividing network coupled to the oscillator for dividing the variable frequency signal to produce an output signal (see abstract). Furthermore, a phase detector coupled to the reference frequency source and to the adjustable dividing network for producing an error signal in accordance with the difference between the fixed frequency signal and the output signal and a filter coupled to the phase detector (see abstract and claim 1).

Although, Dudziak et al. teach an adjustable dividing network coupled to the oscillator and phase

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detector, Dudziak et al. **do not explicitly** teach a variable transfer function element responsive to the detector. **However**, Bickley et al. in an analogous art teach “performing periodic self-calibration” (see col. 2, lines 1-3) and in figure 6 Bickley et al. teach first and second signal processors (42, 44) each receive one of the differential components and processes it according to a respective variable transfer function and the outputs of the processors are input into a synchronous detector (78) where its level is detected to improve the null sensitivity of the receiving system (70) and the output of the synchronous detector is delivered to a controller (50) for use in sensing the null for calibration (see col. 8, lines 34-58). **Therefore**, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the calibrating circuit of Dudziak’s to include a variable transfer function means responsive to the synchronous detector as taught by Bickley et al. for use in sensing the null for calibration. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because it would improve the null sensitivity of the receiving system (see col. 8, lines 48-57).

As per claim 2, Dudziak et al. in view of Bickley et al. teach all subject the matter claimed in claim 1 including Bickley et al. in an analogous art teach “performing periodic self-calibration” (see col. 2, lines 1-3) and in figure 6 Bickley et al. teach first/second signal processors (42, 44) each receive one of the differential components and processes it according to a respective variable transfer function and the outputs of the processors are input into a synchronous detector (78) where its level is detected to improve the null sensitivity of the receiving system (70) and the output of the synchronous detector is delivered to the controller (50) for use in sensing the null for calibration (see col. 8, lines 34-58). Further, Bickley et al. in

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figure 3 teach a signal processor comprising a variable gain amplifier and variable phase shifter wherein the variable gain amplifier includes resistors (see col. 5, lines 21-30).

As per claims **3, 5, 6 and 30**, Dudziak et al. in view of Bickley et al. teach all the subject matter claimed in claims 1 and 29 including Dudziak et al. disclose signal generator including periodic self-calibration, including a reference frequency source for producing a fixed frequency (shaped frequency) signal (see claim 1).

As per claim **4**, Dudziak et al. in view of Bickley et al. teach all the subject matter claimed in claim 1 including Bickley et al. in figure 6 disclosed a calibration switch and when the a self-calibration is initiated by the controller the position of the calibration changed the first position to the second (see col. 8, lines 10-19).

As per claims **7, 8 and 32**, Dudziak et al. in view of Bickley et al. teach all the subject matter claimed in claims 1 and 29 including Dudziak et al. teach phase detector means coupled to the reference frequency source and the dividing network and responsive to the fixed frequency signal and the output signal for producing an error voltage in accordance with the difference between the fixed frequency signal and the output signal (see claim 1). Further, Bickley et al. in figure 6, (see element 78) teach a synchronous detector.

As per claim **9**, Dudziak et al. in view of Bickley et al. teach all the subject matter claimed in claim 1 including Dudziak et al. in figure 3 teach a loop filter coupled to phase detector (see elements 12,18 and claim 2).

As per claims **10, 11, and 31**, Dudziak et al. in view of Bickley et al. teach all the subject matter claimed in claims 1 and 29 including Dudziak et al. in figure 3 teach a loop filter coupled to phase detector (see elements 12 and 18). Dudziak et al. teach a calibrated routine functions

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incrementing the DAC values and checking the phase detector output for a specific value and as an alternative, the routine could be operated by decrementing the DAC values and checking the opposite sense of the voltage comparator.

As per claim 12, Dudziak et al. in view of Bickley et al. teach all the subject matter claimed in claim 1 including Bickley et al. teach that AMI (amplitude modulation interference) components can be canceled by combining two differential output signals from each pair of IF (intermediate frequency) filters into a single-ended signal using a differential amplifier (see col. 4, lines 1-8).

As per claim 13, Dudziak et al. teach or disclose a signal generator including a calibration circuit for providing periodic recalibration of the generator and a reference frequency source for producing a fixed frequency signal (see abstract). Dudziak et al. in figure 3, teach a loop filter coupled to a phase detector (see elements 12,18 and claim 2). Further Dudziak et al. disclose an oscillator (VCO) for producing a variable frequency signal in accordance with a voltage input to the oscillator and an adjustable dividing network coupled to the oscillator for dividing the variable frequency signal to produce an output signal (see abstract). Furthermore, a phase detector coupled to the reference frequency source and to the adjustable dividing network for producing an error signal in accordance with the difference between the fixed frequency signal and the output signal and a filter coupled to the phase detector (see abstract and claim 1). Although, Dudziak et al. teach an adjustable dividing network coupled to the oscillator and phase detector, Dudziak et al. **do not explicitly** teach a variable transfer function element responsive to the detector. **However**, Bickley et al. in an analogous art teach "performing periodic self-calibration" (see col. 2, lines 1-3) and in figure 6 Bickley et al. teach first/second

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signal processors (42, 44) each receive one of the differential components and processes it according to a respective variable transfer function and the outputs of the processors are input into a synchronous detector (78) where its level is detected to improve the null sensitivity of the receiving system (70) and the output of the synchronous detector is delivered to the controller (50) for use in sensing the null for calibration (see col. 8, lines 34-58). **Therefore**, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the calibrating circuit of Dudziak's to include a variable transfer function means responsive to the synchronous detector as taught by Bickley et al. for use in sensing the null for calibration. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because it would improve the null sensitivity of the receiving system (see col. 8, lines 48-57).

As per claims **14, 15 and 28**, Dudziak et al. in view of Bickley et al. teach all the subject matter claimed in claim 13 including Bickley et al. teach that AMI (amplitude modulation interference) components can be canceled by combining two differential output signals from each pair of IF (intermediate frequency) filters into a single-ended signal using a differential amplifier (see col. 4, lines 1-8).

As per claims **16, 26 and 27**, Dudziak et al. in view of Bickley et al. teach all the subject matter claimed in claim 13 including Bickley et al. in an analogous art teach "performing periodic self-calibration" (see col. 2, lines 1-3) and in figure 6 Bickley et al. teach first/second signal processors (42, 44) each receive one of the differential components and processes it according to a respective variable transfer function and the outputs of the processors are input into a synchronous detector (78) where its level is detected to improve the null sensitivity of the

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receiving system (70) and the output of the synchronous detector is delivered to the controller (50) for use in sensing the null for calibration (see col. 8, lines 34-58). Further, Bickley et al. in figure 3 teach a signal processor comprising a variable gain amplifier and variable phase shifter wherein the variable gain amplifier includes resistors (see col. 5, lines 21-30).

As per claims **17, 19, and 20**, Dudziak et al. in view of Bickley et al. teach all the subject matter claimed in claim 13 including Dudziak et al. disclose signal generator including periodic self-calibration, including a reference frequency source for producing a fixed frequency (shaped frequency) signal (see claim 1).

As per claim **18**, Dudziak et al. in view of Bickley et al. teach all the subject matter claimed in claim 13 including Bickley et al. in figure 6 disclosed a calibration switch and when the a self-calibration is initiated by the controller the position of the calibration changed the first position to the second (see col. 8, lines 10-19).

As per claims **21 and 22**, Dudziak et al. in view of Bickley et al. teach all the subject matter claimed in claim 13 including Dudziak et al. teach phase detector means coupled to the reference frequency source and the dividing network and responsive to the fixed frequency signal and the output signal for producing an error voltage in accordance with the difference between the fixed frequency signal and the output signal (see claim 1). Further, Bickley et al. in figure 6 (see element 78) teach a synchronous detector.

As per claim **23**, Dudziak et al. in view of Bickley et al. teach all the subject matter claimed in claim 13 including Dudziak et al. in figure 3 teach a loop filter coupled to phase detector (see elements 12,18 and claim 2).

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As per claims **24 and 25**, Dudziak et al. in view of Bickley et al. teach all the subject matter claimed in claim 13 including Dudziak et al. in figure 3 teach a loop filter coupled to phase detector (see elements 12 and 18). Dudziak et al. teach a calibrated routine functions incrementing the DAC values and checking the phase detector output for a specific value and as an alternative, the routine could be operated by decrementing the DAC values and checking the opposite sense of the voltage comparator.

7. Claims **33-35** rejected under 35 U.S.C. 103(a) as being unpatentable over Bickley et al. (U.S. PN: 6,088,581).

As per claim **33**, Bickley et al. in figure 2 disclose or teach an amplitude modulated interference (AMI) nulling circuitry (32) whereby the AMI circuitry includes a first signal processor (42) and a second signal processor (44) for processing first and second differential output signals from a mixer (24a). The first signal processor (42) includes an adjustable transfer function that is controlled by a controller (50). The controller (50) adjusts the transfer function of the first signal processor (42) to equalize the magnitudes of AMI components in the first and second differential output signals. The first and second differential output signals are then combined in a manner which cancels the equalized interference signal components (see abstract). Further, Bickley et al. teach that a substantial portion of these AMI components can be canceled by combining the two differential output signals from each pair of filters into a single-ended signal using a differential amplifier and if the AMI signal components in each of the two differential output signals were exactly the same, the combination of the signals would perfectly cancel the AMI components and a clean output signal would be sent to the detector

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(see col. 3 last paragraph). Furthermore, Bickley et al. in figure 9 disclose a buffer amplifier comprising an inverting and non-inverting coupled to the first and second resistors (see the IF inputs). Bickley et al. **do not explicitly** teach a variable transfer function elements to the input of the instrumentation amplifier without interrupting normal operation of the voltage difference amplifier. **However**, Bickley et al. teach an adjustment value is updated periodically, or continuously, whether a parameter value change has been detected or not which the method is basically the same as the applicants method since the technique can be used without interruption due to the continuity process. **Therefore**, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to transmit a calibration signal through the variable transfer function elements (equalizers) without interrupting normal operation since Bickley et al's self-calibration means include means for varying a transfer function adjustment value applied to first signal processor while monitoring the receiver's output level to determine a transfer function adjustment value. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because it would be relatively and yet high reliable in operation.

As per claim 34, Bickley et al. in figure 6 teach a receiving system capable of periodic self-calibration includes a calibration switch (72), first and second processors (42,44), a synchronous detector (78) and an amplifier (82) coupled to each other.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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US PN: 6,252,454 Thompson et al.
US PN: 6,285,304 Schweighofer et al.
US PN: 5,877,612 Straw
US PN: 5,990,716 Chen
US PN: 6,262,625 Perner et al.
US PN: 6,046,632 Straw
US PN: 6,160,851 Brown et al.
US PN: 5,481,573 Jacobowitz et al.

9. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham
Esaw Abraham

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Guy J. Lamare
for
Albert DeCady
Primary Examiner